INVITED PAPER

# Designing A Broadband, Highly Efficient, GaN RF Power Amplifier

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*A design approach for a broadband, linear, efficient output back-off mode RF power amplifier (RFPA) emphasizes the importance of minimizing design uncertainties. Using this approach, excellent agreement between modeled and measured performance is achieved with a first-pass design.*

Demand for linear RFPAs covering the frequency range from 1.5 to 2.8 GHz is driving new design methods for broadband, linear and highly efficient RFPAs operating in output back-off mode. Improving efficiency in PAs has long been a challenge for designers, in part due to poor control of harmonic load impedances. The difficulty measuring waveforms at microwave frequencies makes it hard to determine if optimum waveshaping has been achieved. Broadband design adds a challenge when a harmonic of a lower operating frequency lies in the operating band. These inherent difficulties can be compounded by imprecise design techniques, leading to multiple time-consuming and expensive iterations.

In this article, a design flow is described that uses NI AWR Design Environment, specifically Microwave Office circuit design software, as well as a measurement technique for determining the input and output impedances of the matching networks, prior to RFPA turn on. Several approaches to the problems inherent in PA design are presented with the aim of minimizing uncertainty and achieving first-pass success.

The effectiveness of this approach is demonstrated using a commercially available discrete 10 W GaN on SiC, packaged, high electron mobility transistor fabricated with a 0.25 µm process (Qorvo's T2G6000528) and a 20 mil RO4350B printed circuit board. The fabricated RFPA achieves a peak power greater than 40 dBm and a peak drain efficiency greater than 54 percent over its operating bandwidth. In back-off mode, the RFPA achieves an uncorrected linearity of 30 dBc and drain efficiency of 34 percent or higher when driven with a 2.5 MHz, 9.5 dB peak-to-average power ratio (PAPR) COFDM signal in the 2.0 to 2.5 GHz band.

## RFPA DESIGN FLOW

### Device Selection

The first step begins with a thorough device/technology selection process to determine the best candidate device to meet a specific set of criteria prior to the time-consuming tasks of load- and source-pull and network synthesis. Several candidates are acceptable on the basis of claimed frequency and power. In addition to the more common characteristics such as $V_{ds}$, gain, operating frequency and power rating, other parameters such as $C_{ds}$, $C_{gs}$ and transformation ratio are considered.

### Optimal Load Impedance Extraction

Once a device is selected and a nonlinear model obtained, optimal source and load impedances are determined. The required load impedances to achieve maximum power, efficiency and gain—or an acceptable trade-off between these performance metrics—are frequency dependent and vary substantially over the operating bandwidth of a broadband design.

To determine the correct load impedance, a combination of load-pull plotting

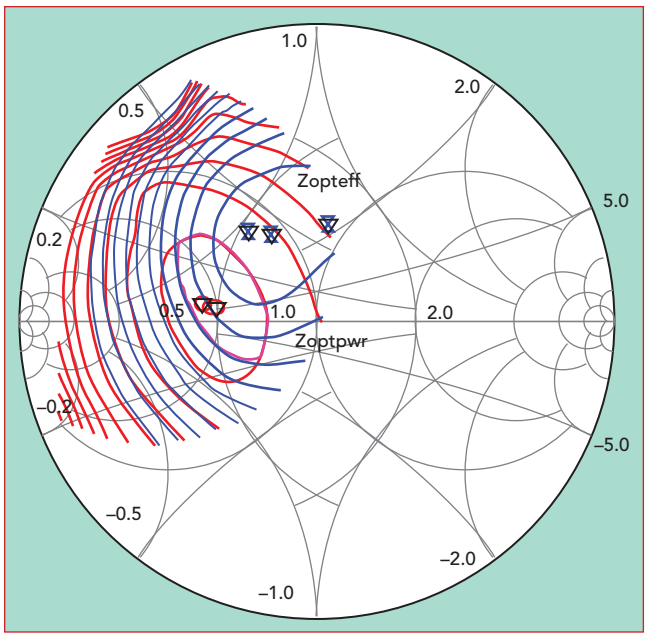


Fig. 1 **Fundamental frequency load-pull analysis showing power (red) and efficiency (blue) contours over the operating bandwidth.**

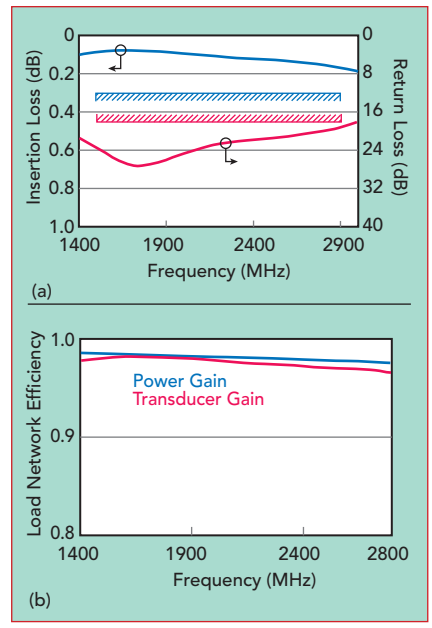


Fig. 2 **Distributed load network loss and match (a) and transducer and operational power gain vs. frequency (b).**

at the fundamental and harmonic frequencies and waveform engineering (circuit design techniques based on shaping the transistor voltage and current waveforms) are performed in Microwave Office. The use of waveform engineering relies on having access to the intrinsic device nodes across the current generator of the device plane, rather than at the package reference plane. Assuming the nonlinear device model provides these nodes, a waveform engineering approach enables the visual observation of voltage and current swing, clipping and amplifier class of operation.

For this example, a load-pull simulation is run at $V_{ds}$ = +28 V and $I_{dq}$ = 90 mA across the operating band, and the impedances for optimal power and efficiency are extracted, with the mid-band results shown in ***Figure 1***. A target load region based on the overlap between $P_{max}$ -1 dB and drain efficiency max ($eff_{max}$) -5 percent is defined. Clearly, the larger this target area is, the easier the matching problem becomes. In this case $P_{max}$ occurs on a tightly-packed clockwise rotating locus over the operating bandwidth, which is helpful in the case of a broadband amplifier. Load-pull is performed at the fundamental frequency due to the broadband nature of the RFPA and consequent difficulties in achieving optimal harmonic terminations[1] without using transmission zeros in the network.[2] Load-pull at the second harmonic is also performed, with a region of high efficiency identified[1] that can be controlled in the network synthesis.

## Network Synthesis

Narrowband RFPAs have the advantage of little variation of the optimal load impedance over their operating bandwidth, making the task of network design less complex. This is not to say that a low fractional bandwidth match is always trivial. Indeed, an investigation of source and load impedances will reveal that for very high performance, the network fundamental impedance must often be precisely controlled to a single gamma point, with significant suboptimal performance penalties if the network locus misses its target load impedance. Precise control of harmonic termination impedances for F and $F^{-1}$ amplifier classes increases the complexity of the task beyond what is required for an average PA design.

In the case of a broadband amplifier, particularly one with high performance specifications, the network is required to control its impedance variation over a far larger fractional bandwidth. After defining optimal impedances and target areas, the load network is developed using a simplified real-frequency technique (SRFT)[3] to design the ideal lumped-element network and convert it to a distributed stepped-impedance format,[4] before performing electromagnetic (EM) simulation. In this example, EM simulation results agree closely with model predictions; however, for less conventional matching topologies, this might not be the case. In general, EM simulation is seen as an important step in reducing uncertainty in the design flow.

One design technique is to represent the conjugate of the optimal impedance as that of a two-terminal generator (port 1), after which the matching network design can be viewed as a problem of reducing the mismatch loss that exists between this complex-valued load and a 50 Ω termination over the amplifier's operating bandwidth. This mismatch can, however, be evaluated at the 50 Ω side (port 2) of the network, as shown in ***Figure 2a***. As a passive network, the output matching circuit has an operating power gain less than 1, equal to its efficiency determined only by internal dissipative loss. The necessarily smaller transducer gain is the product of this efficiency with the effect of loss due to reflection at the input. These quantities are shown as percentage efficiencies in ***Figure 2b***. The efficiency of the load network is calculated to be 96.6 percent at 2800 MHz, close to the value calculated from return loss at the same frequency. For comparison, the operational power gain, which considers purely ohmic loss in the network, is calculated to have an efficiency of 97.7 percent. Although this does not directly include reflection losses, its value does depend on the termination impedances, as these affect the distribution of current and

voltage within the network, hence the copper and dielectric losses, respectively.

Transducer gain is evaluated for a generator whose impedance is the conjugate of the target load impedance seen by the device drain. Although the output is matched for compressed power and efficiency, not for minimum reflection at the drain, the use of a conjugate match is found to agree well with the predicted reduction in compressed power due to imperfect realization of the target load impedance. Thus, the plotted transducer gain is a good measure of the overall quality of the output match.

Achieving an optimal broadband match using this transistor is relatively straightforward for several reasons. First, the transformation ratio is relatively low over the operating bandwidth (about 2:1); second, the load impedance for optimal $P_{max}$ are tightly packed; finally, the optimal impedance varies with increasing frequency in a clockwise rotating locus. The fairly low transformation ratio is a useful criterion favoring the selection of this GaN device for a broadband RFPA application.

### Source Network

Control of source impedance variation over the operating bandwidth is achieved through the use of a bandpass filter network, which also has the advantage of reducing low frequency gain, where the transistor's inherent gain is very high. This particular source impedance matching network is also responsible for improving the amplifier's low frequency stability. The impedance transformation ratio of about 15:1 requires a more elaborate network. Although not used here, matching networks with a positive slope, or equalization, can be conveniently introduced into the source matching circuit, as well.

Stability is achieved using a shunt connected series RC pair adjacent to the input port followed by a series R. Although this is a severe approach, analysis shows the transistor to be potentially unstable in the operating band, and some gain must be sacrificed to achieve unconditional stability from 1 MHz to greater than 6 GHz, where the transistor ceases to have gain ($F_{max}$).

### Waveform Engineering

Waveform engineering[5] is also used to analyze the RFPA, using both the load-pull tuner and, more critically, the realized load network. Recent device models giving access to the voltage and current nodes at the intrinsic current generator plane allow accurate observation of both the V and I waveforms and the dynamic load line (DLL). This enables analysis of clipping and the RFPA mode of operation, as well as the peak voltages and currents generated.

Prior to these nodes being available, the only option was to monitor waveforms at the package plane, which clearly has limitations due to package parasitics. Negation of the parasitic network is feasible, but only if the topology and component values are known and their electrical impact removed through de-embedding during simulation. Although care has been taken to control the second harmonic load impedance, analysis of the waveforms (see ***Figure 3***) shows that the third harmonic impedance is favorable without further optimization.

These waveforms show a peak voltage of less than 60 V and a peak current of less than 1500 mA at 1500 MHz, which are well within device ratings. More significant, in terms of efficiency, is near-ideal class F operation, with the half-wave rectified current waveform exactly 180 degrees out of phase with the voltage waveform and very little voltage/current overlap. Using a DLL analysis, three regions are defined: region A ($V_{min}$ and $I_{max}$), region B ($V_{max}$ and $I_{min}$) and the transition region. Over one period, the waveform remains in region A or B for 63.8 percent of the time, while in the transition region for only 36.2 percent of the period.

## RFPA VALIDATION

To validate the approach, the RFPA was fabricated on Rogers 4350B

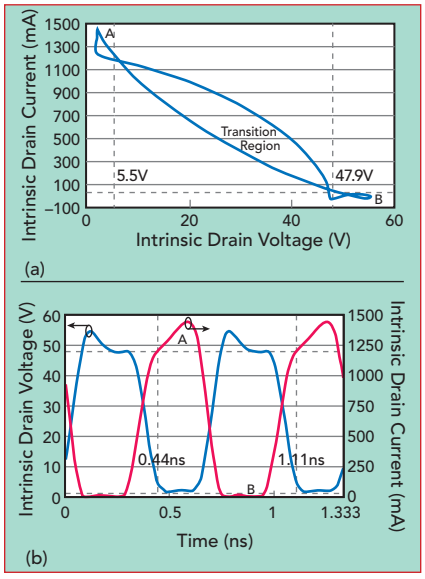


Fig. 3 **DLL (a) and IV waveforms (b) at the intrinsic device nodes, with a 1500 MHz CW signal and 10 W output power.**

20 mil board ($\varepsilon_r$ = 3.48). The circuit was mounted on a jig consisting of three pieces containing the source network (INMAT), load network (OUTMAT) and a copper center section to mount the device (see ***Figure 4***). The device source was soldered down.

## Passive Measurements

Prior to complete assembly, the impedances of the INMAT and OUTMAT circuits, as presented to the transistor tabs, were measured to correlate the modeled and measured datasets. The measured data shows excellent agreement with

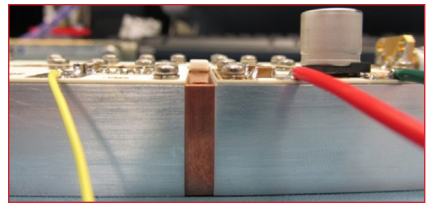

Fig. 4 **Fabricated RFPA.**

the modeled impedance from 1000 to 3000 MHz with no tuning (see ***Figure 5a***). A measurement of the INMAT and OUTMAT circuits over a wider band from 20 MHz to 10 GHz still shows very good agreement between modeled and measured impedance (see ***Figures 5b*** and ***5c***). With the aid of the modular three-piece jig, impedances seen by the device can be measured directly and accurately without using mechanically awkward probes, which can introduce electrical parasitic—notably stray inductance—at the attachment point. The jig is not the production version of the amplifier but is an important step in the design flow, to eliminating uncertainties at each design stage.

## Small-Signal Measurements

Initial small-signal gain measurements used a drain bias of $V_{ds}$ = +28 V and an $I_{dq}$ = 90 mA. Measured and modeled gain and impedance match are closely correlated (see ***Figure 6***) with a small-signal gain greater than 16 dB and an input return loss greater than 7.5 dB over the operating band. The amplifier is stable when subjected to practical stability tests such as varying the drain rail voltage and using an external tuner to vary the source impedance seen by the device.

## Large-Signal Measurements

Large-signal measurements used a drain bias of $V_{ds}$ = +28 V and an $I_{dq}$ = 90 mA. A continuous wave signal source was fed to the amplifier through a driver amplifier. RF input and output power measurements were corrected for any compression in the driver. Power gain, drain efficiency and power delivered to the load were measured at 3 dB compression. The modeled results show a maximum $P_{3dB}$ of 41 dBm, maximum drain efficiency of 63.2 percent and a maximum gain of 16.4 dB. The measured results show a $P_{3dB}$ of 40.6 dBm, maximum drain efficiency of 59.1 percent and a maximum gain of 15.7 dB (see ***Figure 7***). The RFPA delivers more than 10 W down to 1300 MHz and up to 2900 MHz, extending its range to a fractional bandwidth of 76.2 percent.

To evaluate efficiency in output back-off mode and intermodulation sideband performance, a 2.5 MHz channel bandwidth COFDM signal with 9.5 dB PAPR was used over the band from 2.0 to 2.5 GHz. As a single-ended amplifier at 34.5 dBm output power, the average efficiency was 34 to 35.9 percent, with a linearity of 30 dBc measured ±1.25 MHz about the center fre-

quency (see ***Figure 8***). Similar results were obtained in the band from 1.805 to 1.88 GHz using a WCDMA test signal with PAPR = 7.8 dB.

A balanced version of the amplifier is under construction. Including imperfect hybrids, it is predicted to achieve +37 dBm with an average efficiency of approximately 34 percent and a linearity of 30 dBc at ±1.25 MHz from the center frequency. Linearity could be improved using linearization techniques such as digital predistortion or envelope tracking. Achieving high efficiency at signal peaks enables operation at greater peak compression, so the amplifier can be operated at higher

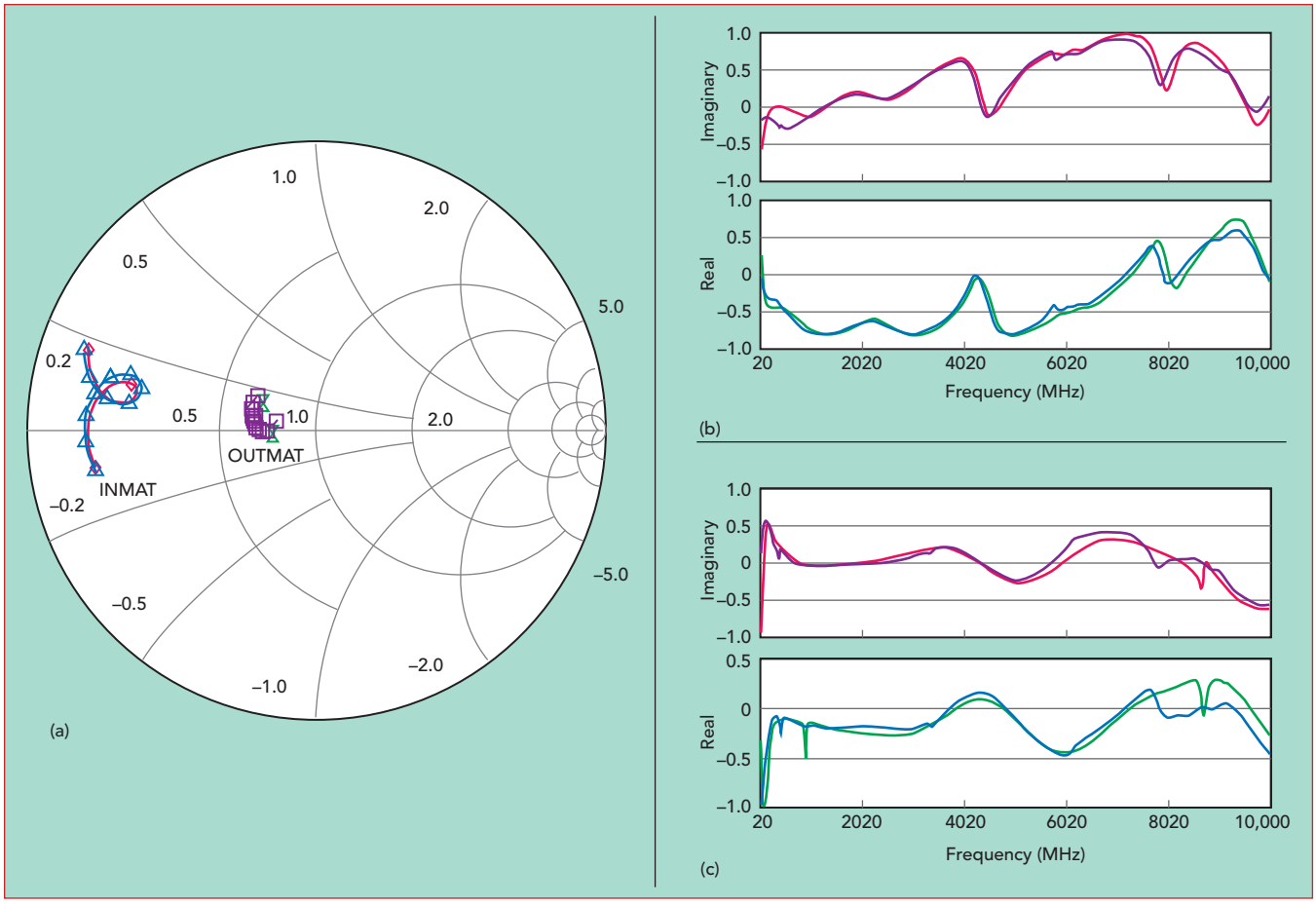


Fig. 5 5 Measured vs. modeled INMAT and OUTMAT impedances from 1000 to 3000 MHz (a); measured vs. modeled impedances from 20 MHz to 10 GHz for the INMAT (b) and OUTMAT (c) circuits.

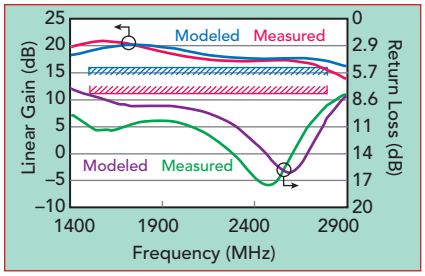


Fig. 6 **Modeled vs. measured small-signal gain and input return loss.**

relative power over the whole dynamic range. Hence, efficiency and linearity are improved even on high PAPR signals.

## CONCLUSION

An approach for the design of broadband, linear and highly efficient RFPAs minimizes uncertainty to achieve first-pass success. The design methodology comprises four stages: device selection using qualitative and quantitative analysis, optimization of load and source impedance matching networks using load- and source-pull, passive network synthesis including EM verification and waveform engineering using intrinsic voltage and current nodes. Together, these techniques provide a proven systematic approach to designing the entire RFPA.

A measurement technique for fabricated source and load networks, enabling comparison of modeled and measured impedances at the transistor tabs, has also been demonstrated using a three-piece jig. Passive network synthesis, using an SRFT technique combined with analysis using mismatch loss and transducer power gain, provides a broadband match with relatively simple matching networks.■

## ACKNOWLEDGMENTS

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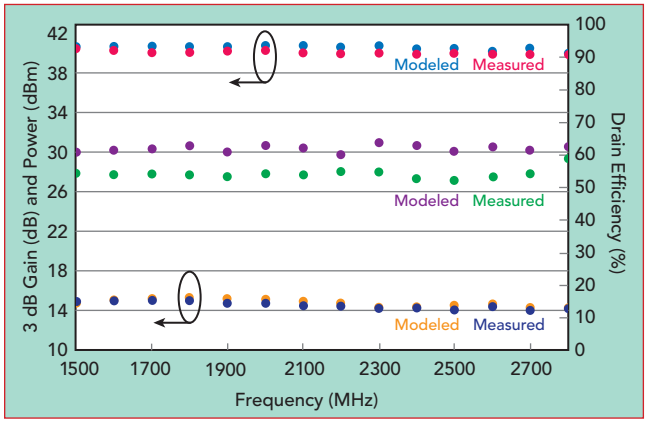


Fig. 7 **Modeled vs. measured large-signal CW power, gain and efficiency.**

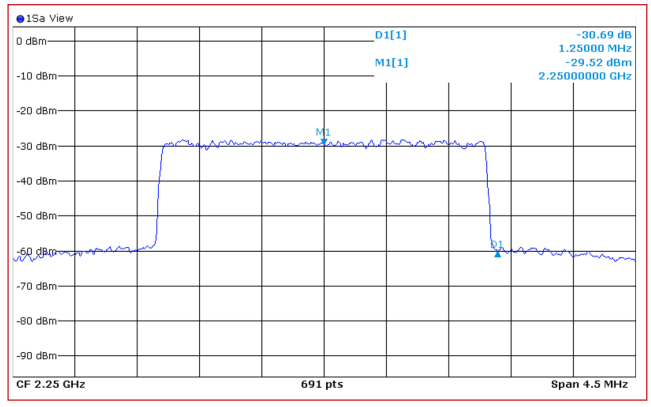


Fig. 8 **Single-ended amplifier intermodulation performance with a 2.5 MHz, 9.5 dB COFDM signal.**